ABSTRACT OF THE DISCLOSURE

Testing capability for an integrated circuit having more than one serializer/deserializer (SERDES) block includes embedding a tester within each block, so that the blocks can be tested independently and concurrently. In one embodiment, a tester includes a functional test controller (FTC) for mode setting and a functional test interface (FTI) for implementing the test procedures. The FTI of each tester is inserted between the SERDES of the same block and core processing logic that is also embedded within the integrated circuit. The FTCs are all interconnected via a test bus that is connected to an input/output controller (IOC) for communication between the testers and an external source, such as a personal computer. Optionally, a built-in-self-tester (BIST) state machine is connected to the test bus.